

CLMPTO

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CLAIMS 1-27 (CANCELLED)

Claim 28 (Previously Presented): A semiconductor device, comprising:

- a substrate;
 - a gate electrode provided on said substrate;
 - a diffusion region formed in said substrate adjacent to said gate electrode;
 - a side-wall insulation film formed on a side wall of said gate electrode;
 - a self-aligned contact hole defined by said side-wall oxide film and exposing said diffusion region; and
 - a silicide region formed selectively on a surface of said diffusion region;
- ✓ wherein said semiconductor device further includes;
- a first insulation film provided on said gate electrode so as to cover said side wall oxide film partially;
 - a second insulation film having a composition different from a composition of said first insulation film and provided on said first insulation film;
 - an interlayer insulation film deposited on said second insulation film;
 - a contact hole formed in said interlayer insulation film, said contact hole extending through said first and second insulation films and exposing said self-aligned contact hole;
 - said first insulation film contains H₂O with an amount smaller than about 2.4 wt%.

Claim 29 (Original): A semiconductor device as claimed in claim 28, wherein said first insulation film contains H_2O with an amount of about 1.1 wt % or less

Claim 30 (Canceled)

Claim 31 (Previously Presented): A semiconductor device as claimed in claim 28, further comprising a conductor pattern contacting with said diffusion region and said gate electrode such that said conductor pattern extends along a surface of said side wall oxide film.

Claim 32 (Canceled)

Claim 33 (Previously Presented): A semiconductor device as claimed in claim 28, further comprising another silicide region formed selectively on a surface of said gate electrode.

CLAIMS 34-42 (CANCELLED)

Claim 43 (New): A semiconductor device, comprising:

a substrate;

a gate electrode provided on said substrate;

a diffusion region formed in said substrate adjacent to said gate electrode;

a side-wall insulation film formed on a side wall of said gate electrode;

a self-aligned contact hole defined by said sidewall oxide film and exposing said diffusion region;

a silicide region formed selectively on a surface of said diffusion region;

a first insulation film provided on said gate electrode so as to cover said side wall oxide film partially;

a second insulation film having a composition different from a composition of said first insulation film and provided on said first insulation film;

an interlayer insulation film deposited on said second insulation film; and

a contact hole formed in said interlayer insulation film, said contact hole extending through said first and second insulation films and exposing said self-aligned contact hole,

wherein said first insulation film is formed by a plasma CVD process with a plasma power of 100W or less and contains H_2O with an amount smaller than about 1.1 wt%, and said first insulation film has a refractive index of 1.5 or less.